Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of managing traffic over a network comprising:
receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;
performing a policing function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit;
performing a congestion control function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core;
performing a scheduling function in a third core of the digital signal processing integrated circuit, wherein the third core processes data generated by the second core; and
performing a shaping function in a fourth core of the digital signal processing integrated circuit, wherein the fourth core processes data generated by the third core.

[c2] A method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;
performing a first traffic management function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit; and
performing a second traffic management function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core.

[c3] The method of claim 2 wherein a traffic management function comprises sorting the traffic by class of service, policing traffic to not exceed boundary of a bandwidth of the channel, and scheduling traffic.

[c4] The method of claim 3 wherein the scheduling traffic is based on priority queuing, first in first out queuing, class based queuing, round robin, waiting round robin, earlier deadline first, weighted fair queue, deficit round robin, or modified deficit round robin.

[c5] The method of claim 2 wherein there is no direct communication path between the first core and the second core.

[c6] The method of claim 2 wherein the data generated by the first core is passed to the second core using a mail-box.

[c7] The method of claim 2 wherein the first core and second core are synchronized using an interrupt mechanism with a plurality of timers.

[c8] A method of managing traffic over a network comprising:
receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;
performing a first portion a traffic management function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit; and
performing a second portion the traffic management function on the incoming traffic to the digital signal processing integrated circuit in a second core of the digital signal processing integrated circuit,
wherein the first and second portions of the traffic management function are performed in parallel by the first and second cores of the digital signal processing integrated circuit.

[c9] A method of managing traffic over a network compris-

ing:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;

performing a first traffic management function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit;

performing a first portion of a second traffic management function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core; and

performing a second portion of the second traffic management function in a third core of the digital signal processing integrated circuit,

wherein the first and second portions of the second traffic management function are performed in parallel by the second and third cores of the digital signal processing integrated circuit.

[c10] A system comprising a digital signal processing integrated circuit having at least 128K bytes of on-chip memory, wherein the digital signal processing integrated circuit receives a first flow and a second flow of incoming traffic over a network, and the digital signal processing integrated circuit determines whether the first flow

or second flow is next to be processed.

[c11] A system comprising:
a network processor receiving incoming flows from a network;
a digital signal processing integrated circuit, coupled to the network processor, having at least 128K bytes of on-chip memory, wherein the digital signal processing integrated circuit receives a first flow and a second flow of incoming traffic from the network processor, and the digital signal processing integrated circuit communicates to the network processor which of the first flow or second flow is to be processed next.

[c12] The system of claim 11 wherein the on-chip memory has at least 256K bytes of on-chip memory, at least 512K bytes of on-chip memory, or at least 1 megabyte of on-chip memory.

[c13] The system of claim 12 wherein the digital signal processing integrated circuit consumes less than about 2.0 watts.

[c14] The system of claim 12 wherein the digital signal processing integrated circuit has less the about 532 pins, or less than about 650 pins.

[c15] A method of managing traffic over a network compris-

ing:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory;

performing traffic management function for a first layer of the network using a first core of the digital signal processing integrated circuit; and

performing traffic management function for a second layer of the network using a second core of the digital signal processing integrated circuit.

[c16] A system comprising:

a plurality of incoming flows and a plurality of connections;

a network processor receiving the incoming flows and capable of linking one of the incoming flow to one of the connections; and

a digital signal processing integrated circuit, coupled to the network processor, wherein the digital signal processing integrated circuit selects one of the plurality of flows and instructs the network processor to connect a selected flow to a first connection, the digital signal processing integrated circuit comprising:

a first core managing a first layer of traffic management of the incoming flows from the network processor;

a second core managing a second layer of traffic man-

agement of the incoming flows from the network processor; and

a plurality of bits to communicate between layers of the first core and the second core.

[c17] A method of managing flows over a network comprising:

providing a class of service memory location, wherein a bit location of the class of service memory location represents a class of service;

identifying a first class of service of a first flow;

setting a first bit location in the class of service memory location associated with the first class of service in the class of service memory location;

identifying a second class of service of a second flow, wherein the second class of service of the second flow is different from the class of service of the first flow;

setting a second bit location associated with the second class of service, wherein when the second class of service is greater than the first class of service, the second bit location is in a first direction with respect of the first bit location, and when the second class of service is less than the first class of service, the second bit location is in a second direction with respect of the first bit location;

executing an instruction of the digital signal processor integrated circuit to determine in the class of service

memory location a bit in a first state of the class of service memory location starting from one side of the class of service memory location; and

processing the first flow before or after the second flow based on relative locations of the first bit and second bit in the class of service memory location.

[c18] The method of claim 17 wherein the first state is a 1.

[c19] The method of claim 17 wherein the first state is a 0.

[c20] The method of claim 17 wherein the first direction is a left direction and the second direction is a right direction.

[c21] The method of claim 17 wherein the first direction is a right direction and the second direction is a left direction.

[c22] The method of claim 17 wherein executing an instruction of the digital signal processor integrated circuit starts from a left side of the class of service memory location and proceeds in a right direction.

[c23] The method of claim 17 wherein executing an instruction of the digital signal processor integrated circuit starts from a right side of the class of service memory location and proceeds in a left direction.

[c24] The method of claim 17 wherein the class of service memory location is a register of the digital signal processor integrated circuit.

[c25] The method of claim 17 wherein the instruction returns an integer representing a number of consecutive 0s from the one side of the class of service memory location.

[c26] The method of claim 25 wherein the instruction excludes counting a sign bit.

[c27] The method of claim 17 wherein the instruction returns an integer representing a number of consecutive 1s from the one side of the class of service memory location.

[c28] The method of claim 17 wherein the instruction returns an integer representing a position of a 1 bit from the one side of the class of service memory location.

[c29] The method of claim 17 wherein the instruction returns an integer representing a position of a 0 bit from the one side of the class of service memory location.

[c30] A system comprising a line card, having a digital signal processor integrated circuit, operating using the method of claim17.

[c31] A method of processing flows of a network comprising:

providing an integrated circuit having a first digital signal processor core and a second digital signal processor core;
executing in the first digital signal processor core a first set of instructions on a first flow;
setting a first flag to indicate the completion of the first set of instructions; and
after the first flag is set, executing in the second digital signal processor core a second set of instructions on the first flow.

[c32] The method of claim 31 setting a second flag to indicate the initiation of the second set of instructions on the first flow.

[c33] The method of claim 32 after the second flag is set, executing in the first digital signal processor core the first set of instructions on a second flow.

[c34] The method of claim 32 after the second set of instructions have completed on the first flow, resetting the first flag.

[c35] The method of claim 32 wherein the second flag is stored in second mailbox memory location.

[c36] The method of claim 32 wherein the first and second flags are stored in a mailbox memory location.

[c37] The method of claim 31 wherein the first flag is stored in a first mailbox memory location.

[c38] A system comprising a line card, having a digital signal processor integrated circuit, operating using the method of claim 31.

[c39] A method of processing flows of a network comprising:
providing an integrated circuit having a first digital signal processor core and a second digital signal processor core;
using the first digital signal processor core to enable a master timer circuit, wherein the master timer circuit enables operation of a first and second timer circuits;
providing a first interrupt to the first digital signal processor core using the first timer circuit;
providing a second interrupt to the second digital signal processor core using the second timer circuit; and
processing a first flow using the first digital signal processor core and second digital signal processor core operating in the same clock domain.

[c40] The method of claim 39 wherein the step of processing a first flow using the first digital signal processor core and second digital signal processor core operating in the same clock domain is replaced by processing a first flow

using the first digital signal processor core and a second flow using second digital signal processor core operating in the same clock domain.

[c41] The method of claim 39 wherein the first digital signal processor core and second digital signal processor core operation at using clocking having the same phase and frequency.

[c42] The method of claim 39 further comprising:
upon receiving the first interrupt, executing in the first digital signal processor core instructions starting at a first memory location; and
upon receiving the second interrupt, executing in the second digital signal processor core instructions starting at the first memory location.

[c43] A system comprising a line card, having a digital signal processor integrated circuit, operating using the method of claim 39.

[c44] A network management system comprising:
a backplane;
a first card, coupled to the backplane, comprising a first digital signal processor integrated circuit to process packet flows of the network management system directed to the first card; and

a second card, coupled to the backplane, comprising a second digital signal processor integrated circuit to process packet flows of the network management system directed to the second card, wherein the backplane provides a communication path between the first and second card.